https://doi.org/10.46335/IJIES.2025.10.9.4 e-ISSN: 2456-3463
Vol. 10, No. 9, 2025, PP. 16-21

International Journal of Innovations in Engineering and Science, www.ijies.net

Low Power VLSI Design – A Literature Survey

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0009-0007-0515-5297, 0009-0003-2174-5669, 0009-0008-0108-6615

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Received on*: 18 May,2025* ***Revised on****: 24 June,2025* ***Published on****: 26 June,2025*

Abstract *-Low power has emerged as a principal theme in today's world of electronics industries. Power dissipation has become an important consideration as performance and area for VLSI Chip design. With shrinking technology reducing power consumption and over all power management on chip are the key challenges below 100nm due to increased complexity. For many designs, optimization of power is important as timing due to the need to reduce package cost and extended battery life. For power management leakage current also plays an important role in low power VLSI designs. Leakage current is becoming an increasingly important fraction of the total power dissipation of integrated circuits.*

This paper describes about the various strategies, methodologies and power management techniques for low power circuits and systems. Future challenges that must be met to designs low power high performance circuits are also discussed.

Keywords: *VLSI, Low power, chip, package, scaling*

I. INTRODUCTION

The advantage of utilizing a combination of low-power components in conjunction with low power design techniques is more valuable now than ever before. Requirements for lower power consumption continue to increase significantly as components become battery powered, smaller and require more functionality. In the past the major concerns for the VLSI designers were area, performance and cost. Power consideration was the secondary concerned. Now a day's power is the primary concerned due to the remarkable growth and success in the field of personal computing devices and wireless communication system which demand high speed computation and complex functionality with low power consumption. The motivations for reducing power consumption differ application to application. In the class of micro-powered battery-operated portable applications such as cell phones, the goal is to keep the battery lifetime and weight reasonable and packaging cost low. For high performance portable computers such as laptop the goal is to reduce the power dissipation of the electronics portion of the system to a point which is about half of the total power dissipation. Finally for the high performance no battery- operated system such as workstations the overall goal of power minimization is to reduce the system cost while ensuring long term device reliability.

For such high-performance systems, process technology has driven power to the fore front to all factors in such designs. At process nodes below 100 nm technology, power consumption due to leakage has

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joined switching activity as a primary power management concern.

There are many techniques [1] that have been developed over the past decade to address the continuously aggressive power reduction requirements of most of the high performance. The basic low-power design techniques, such as clock gating for reducing dynamic power, or multiple voltage thresholds (multi-Vt) to decrease leakage current, are well-established and supported by existing tools [2].

II. LITERATURE REVIEW

The continuing demand for higher performance and smaller form factors in electronic devices has necessitated the development of low power design techniques in Very Large-Scale Integration (VLSI). As devices become increasingly miniaturized, power consumption has become one of the most critical design constraints. The need for low power designs is driven by several factors including energy efficiency, thermal management, portability, and battery life, particularly for mobile and IoT devices. This literature review surveys the most relevant low-power design techniques in VLSI, focusing on circuit, architectural, and system-level approaches.

III. METHODOLOGY

Supply Voltage Scaling Voltage has a quadratic effect on dynamic power. Therefore, choosing a lower power supply significantly reduces power consumption. As many transistors are operating in a velocity-saturated regime, the lower power supply may not reduce performance as much as long-channel models predict. The chip may be divided into multiple voltage domains, where each domain is optimized for the needs of certain circuits.[3] In VLSI, power consumption is composed of two main types: dynamic power and static (or leakage) power. Dynamic power is primarily due to the switching activity in transistors and can be reduced effectively by decreasing the supply voltage. The relationship of dynamic power consumption with supply voltage can be expressed by the equation:

$$P_{dynamic} = \alpha C V_{DD}^2 f$$

where: • αis the switching activity factor, • C is the load capacitance, • VDD is the supply voltage, and • f is the operating frequency. In this equation, power consumption is proportional to the square of the supply voltage (Vdd2). Therefore, a 10% reduction in Vdd can reduce dynamic power by roughly 19%, making supply voltage scaling a highly effective means of power reduction.

3.2 Challenges in supply voltage scaling -A factor of two reduction in supply voltage yields a factor of four decrease in energy. Theoretical lower limit of supply voltage of CMOS circuit is 0.2V. As supply voltage is lowered delay increases leading to dramatic reduction in performance. Objective of SVS is to scale supply voltage without compromise performance.[9] Overall, while supply voltage scaling is effective for reducing power, it requires careful management of performance, reliability, and design trade-off.

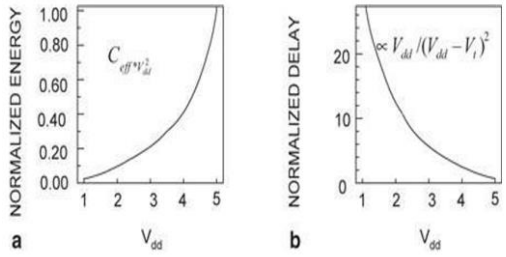

Figure 3.1: Relation between Energy and Delay

Figure 3.1

3.3 Constant Field Scaling in VLSI

Design Constant field scaling is a classical approach in VLSI design used to achieve transistor miniaturization while maintaining or improving performance and reducing power consumption. As transistor sizes shrink with each new technology node, constant field scaling ensures that the electric field within a transistor remains approximately constant, thereby preserving device reliability and preventing performance degradation due to excessive electric fields. This method has been widely used in the semiconductor industry to enable smaller, faster, and more power-efficient devices. The principle of constant field scaling is straightforward: when transistor dimensions (e.g., channel length, width, and oxide thickness) are scaled down by a factor, SSS, other associated parameters (such as supply voltage Vdd, threshold voltage Vth, and doping concentrations) are also scaled to ensure that the electric field across the transistor remains unchanged. This keeps the device consistent with the original design, allowing it to operate reliably despite its reduced size.

https://doi.org/10.46335/IJIES.2025.10.9.4 e-ISSN: 2456-3463
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3.3.1 Key Parameters in Constant Field Scaling In constant field scaling, all critical device parameters are scaled by the same factor, SSS, according to the following rules [9]: 1. Linear Dimensions: Channel length, width, and oxide thickness are scaled by 1/S. 2. Supply Voltage (Vdd): Scaled by 1/S, reducing the power consumption. 3. Doping Concentration: Scaled by S to ensure that threshold voltage and other electrical characteristics are preserved. 4. Threshold Voltage (Vth): Scaled by 1/S, maintaining consistent transistor switching characteristics. This systematic scaling of parameters ensures that the internal electric field (EEE) within the transistor remains nearly constant. E= Vdd /L

3.3.2 Benefits of Constant Field Scaling

1. Reduced Power Consumption: Since power consumption is proportional to the square of the supply voltage (Vdd), scaling down Vdd reduces dynamic power significantly. 2. Higher Device Density: By scaling down the transistor dimensions, more devices can be packed into a given area, leading to higher circuit density and more complex integrated circuits.

3.4 Clock Gating in VLSI Design The commonly used register transfer level (RTL) in the optimization of the reduction of the power dynamics is the Clock gating]. This is because this technique is only applied to the clock modules which instantly working by providing the additional support to the currently existing synchronous circuits in pruning the clock tree thus shutting down the power consumption for the idle circuit in the system. This adoption of this technique can help in the reduction of the dissipation of power in the clock distribution network.

3.4.1 How Clock Gating Works In typical digital circuits, a clock signal is distributed to various flip-flops, latches, and registers. Even when certain parts of a circuit are idle (not processing data), these elements still receive the clock signal, resulting in power consumption due to unnecessary switching. Clock gating reduces this consumption by inserting logic gates, typically an AND or OR gate, in the clock path. These logic gates selectively enable or disable the clock signal based on a control signal (known as the enable signal) that indicates whether a circuit block needs to be active or idle.

The basic mechanism involves: 1. Clock Enable Signal: A control signal that determines if the clock should be delivered toa particular block. When this signal is "low," the clock is disabled for that block, stopping unnecessary toggling. 2. Gating Logic: Usually an AND gate (for a positive-edge-triggered clock) or an OR gate (for a negative-edge-triggered clock), which gates the clock based on the enable signal.

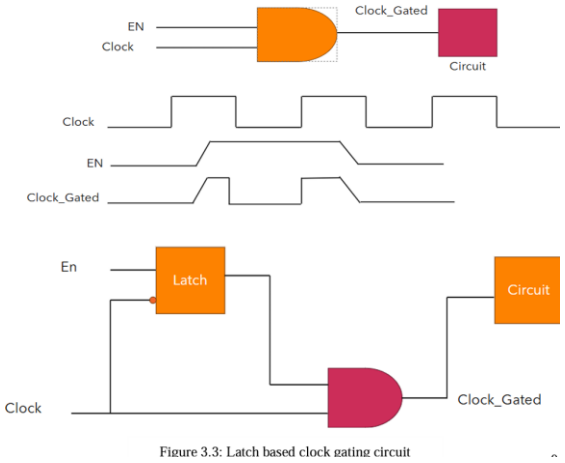

Figure 3.3: Latch based clock gating circuit

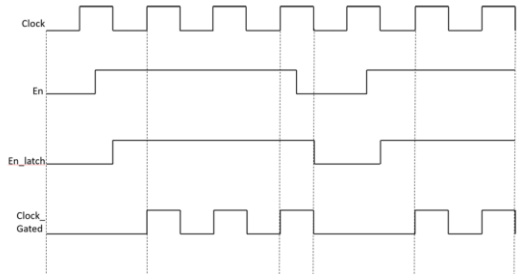

Figure 3.4: Latch based clock gating output

Figure 3.4.1

3.4.2 Types of Clock Gating-1. Synthesis-based Clock Gating: This is an automatic approach where the synthesis tools add clock gating logic based on opportunities identified in the design, such as redundant switching in registers2. Latch-based Clock Gating: This technique involves using a latch to hold the gating condition and applies it directly to the clock signal.3. Integrated Clock Gating Cells: Many modern VLSI libraries provide integrated clock gating cells that combine clock gating logic (such as AND/OR gates) with built-in glitch protection.

3.4.3 Benefits of Clock Gating

1. Reduced Dynamic Power: Clock gating is one of the most effective techniques for reducing dynamic power, as it directly targets the main power-consuming signal in digital circuits. 2. Optimized Power Efficiency: By disabling clock signals to inactive circuit blocks, clock

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gating prevents unnecessary switching, resulting in lower overall power consumption.

3.5 Power Gating

During normal operation, SLEEP = 0. Both the PMOS and NMOS Sleep Transistors (in blue and green respectively) are ON. And we have Virtual Power Rails and Virtual Ground which ensure normal circuit operation. However, during periods of low activity, SLEEP = 1. Hence the Sleep Transistors tum OFF. And a direct path from power rails to ground is broken and hence no leakage power is dissipated due to the Pull-up and Pull-down networks. During normal operation, Sleep Transistors contribute to some extra leakage power because they are still ON. Though, the leakage power due to these two transistors would be extremely small compared to that of the Pull-up and Pull-down networks, nevertheless, these transistors are custom designed in a way such that they have high Vt (the threshold voltage) to reduce any excess leakage power during normal mode of operation.

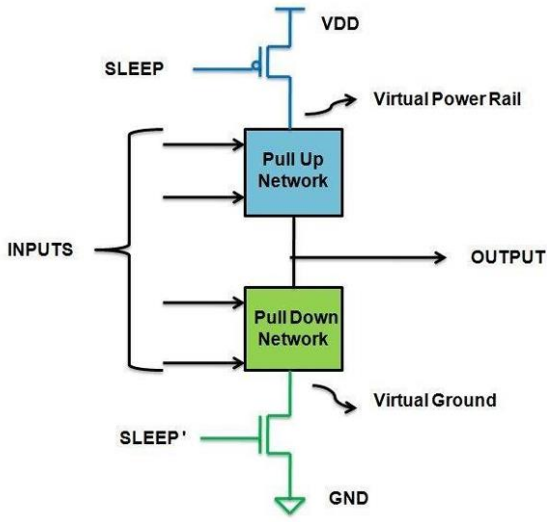

Figure 3.5: Basic power gating circuit

Figure 3.5

3.5.1 Working Phases of Power Gating

The easiest way to reduce static current during sleep mode is to turn off the power supply to the sleeping blocks. This technique is called power gating.

1. Power-on (Active Mode): In this mode, the sleep transistor is turned on, allowing the power supply (Vdd) to flow into the functional block of the circuit. The sleep transistor essentially acts as a low-resistance path, and the block operates as usual.

2. Power-off (Sleep Mode) In this mode, the sleep transistor is turned off. This creates an open circuit between the power supply and the functional block, essentially cutting off the power to the block and reducing leakage currents.

3.6 Dynamic Voltage and Frequency Scaling (DVFS) Dynamic Voltage and Frequency Scaling has emerged as a versatile technique for optimizing power consumption in processors. Initially employed in desktop and server environments, DVFS has garnered attention for its adaptability to the dynamic workload's characteristic of IoT devices. DVFS enables real-time adjustments to the operating voltage and frequency of a processor based on the current computational requirements. This dynamic tuning ensures that the processor operates at an optimal point on the power performance curve, minimizing energy wastage during periods of low workload and maximizing performance during peak demand.

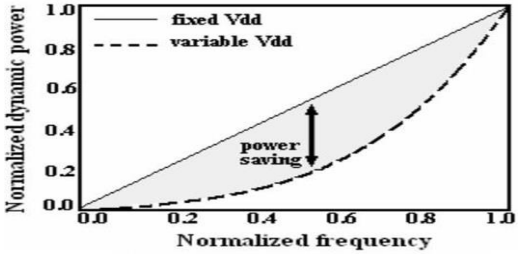

Figure 3.6: Power VS Frequency

Figure 3.6

3.6.1 How DVFS Works DVFS works by scaling two key parameters: 1. Operating Frequency (f): The frequency at which the circuit operates (measured in Hz). The frequency of operation controls how quickly a processor or circuit can perform operations. Higher frequencies lead to higher performance, but also increase power consumption due to the increased number of switching events per unit time. 2. Supply Voltage (Vdd): The voltage that powers the circuit. power consumed by a digital circuit is proportional to both the frequency of operation and the square of the supply voltage. Lowering the voltage reduces dynamic power consumption, but may also reduce the performance capability.

3.6.2 Key Principles of DVFS

1. Power-Performance Trade off: There is a trade between power consumption and performance. Lowering the frequency and voltage reduces power consumption, but can also degrade performance

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2. Dynamic Scaling: DVFS allows the voltage and frequency to be adjusted in real-time based on the workload and performance requirements.
3.6.3 Benefits of DVFS Several studies highlight the tangible benefits of integrating DVFS into the VLSI architecture of IoT devices. can operate in remote or inaccessible locations for extended durations, making them more practical for diverse applications1.Trade-off between Power and Performance: Achieving an optimal balance between power efficiency and performance is a perpetual challenge. Aggressive power saving techniques might lead to a reduction in processing speed and overall system performance.2. Dynamic Workload Variations: IoT applications often experience dynamic and unpredictable workloads. Designing a VLSI architecture that can efficiently adapt to these variations without sacrificing power efficiency poses a significant challenge.
3.7 Sleep Mode Sleep mode is a widely used technique in VLSI (Very-Large-Scale Integration) design to minimize power consumption, particularly in systems where different components may be idle or inactive at various times. By selectively turning off power to specific components (or entire blocks) when they are not in use, sleep mode helps to significantly reduce static power (leakage) and sometimes dynamic power consumption. This is especially important for battery-powered and mobile devices, where energy efficiency is crucial.

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3.7.1 Sleep Mode Types

1. Idle Mode- In idle mode, a block is not performing any useful computation but is still powered on. This is often used in communication systems, where a block might not be processing data but still needs to be ready for quick activation.

2. Standby Mode- In standby mode, the system is partially powered down, meaning that some components of the circuit are turned off while others remain active. For instance, in multi-core processors, cores that are not actively processing data can be powered down while the active cores continue to function.

3. Deep Sleep Mode- Deep sleep mode involves completely turning off power to certain sections of the circuit (or even the entire chip), resulting in the lowest possible power consumption.

3.7.2 Benefits of Sleep Mode in VLSI

1. Reduced Static Power: Static power (mainly due to leakage currents) becomes a dominant factor as semiconductor technology scales down to smaller process nodes (like 7 nm, 5 nm). By turning off power to idle blocks or entire sections of the chip, sleep mode helps reduce these leakage currents and thus lowers overall power consumption.

2. Energy Efficiency: Sleep mode allows components to conserve energy during idle periods. This is especially important for battery-powered devices such as smart phones, laptops, and IoT devices, where saving power during inactive states directly contributes to longer battery life.

3.7.3 Challenges in Implementing Sleep Mode

1. Wake-up Latency: One of the main challenges of using sleep mode is the wake-up latency. When a component is powered down, there can be a delay in returning to full functionality. This latency is the time it takes for the system to re-enable the power supply, re-initialize the block, and resume normal operations.

2. State Preservation: When a block enters sleep mode, it may lose its current state (e.g., register contents, memory data) requiring mechanisms to save and restore the state 19 during transitions.

3. Power Gating Complexity: The design of sleep transistors and power gating logic adds complexity to the chip's architecture. It's crucial to ensure that the sleep transistors do not themselves consume significant power or add parasitic capacitance that

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may undermine the power-saving benefits of sleep mode.

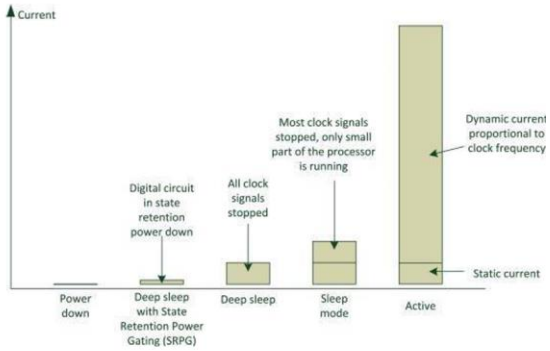

Figure 3.7: Different Sleep Modes

Figure 3.7

IV.APPLICATION

1.ClockGating-Applications:
Microprocessors, FPGAs, embedded systems, SoCs. Purpose: Reduces dynamic power by turning off clocks to inactive parts of the circuit.
2. Power Gating: Applications: Multi-core processors, SoCs, mobile devices, high performance computing. Purpose: Cuts off power to unused blocks, reducing static leakage power.
3.Constant-FrequencyScaling: Applications: Low-power embedded systems, real-time systems, IoT devices. purpose: Lowers voltage while keeping frequency constant, reducing power consumption.
4. DVFS (Dynamic Voltage and Frequency Scaling): Applications: Mobile devices, laptops, servers, high-performance computing. Purpose: Dynamically adjusts both voltage and frequency to optimize power and performance

V. CONCLUSION

The need for lower power systems is being driven by many market segments. Unfortunately designing for low power adds another dimension to the already complex design problem and the design has to be optimized for power as well as Performance and Area. In conclusion various issues and major challenges regarding low power designs are: -

1. Technology Scaling: - It relates with the following factors like: Capacitance per node reduces by 30%, Electrical nodes increase by 2X, die size grows by 14% (Moore's Law), Supply Voltage reduces by 15% and Frequency Increases by 2X. To meet these issues relatively 2.7 X active power will increase.

2. Leakage power: - To meet frequency demand Vt will be scaled which results high leakage power. A low voltage / low threshold technology and circuit design approach, targeting supply voltage around 1V and operating with reduced thresholds. 3. Dynamic power management techniques, varying supply voltage and execution speed according to the activity measurement.
4. Low power interconnect, using advance technology, reduced swing or activity approach.
5. Development of power conscious techniques and tools for behave synthesis, logic synthesis and layout optimization.
6. Power saving techniques that recycle the signal energies using the adiabatic switching principals rather them dissipating them as a heat and promising in certain applications where speed can be trades for low power.

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