Impact Factor Value 4.046 **e-ISSN: 2456-3463**
International Journal of Innovations in Engineering and Science, Vol 4, No.10,2019
National Level Technical Paper Presentation- PHOENIX-19
Organized by Godavari College of Engineering, Jalgaon - 425003
www.ijies.net

Studies in New Architecture for Real-time Control Applications

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Abstract—
Real world automatic control systems were initially based on analogue electronics. With the advent of digital electronics more sophisticated control laws with advanced features were available. In this way, the demand for applications in real time in today's scenario has increased. In this work, an effort to study the new architectures of control systems in real time has been made. The system is the industrial DC motor carried out from design point of view using delta sigma modulator, the controller or processor designing implemented using 1 bit processing which require less silicon footprint.

Keywords*— automatic control system, control laws, real time, industrial DC motor, delta sigma modulator, 1 bit processing, silicon footprint.*

1. INTRODUCTION

Any physical parameter, measured with the help of sensor is of the order of mV and is analog in nature. This signal is of so low strength that it is difficult to interpret the exact information about the physical quantity being measured. Practically, further processing of the signal has been required in order to avoid the effects of noise, stability, drift and other elements that may harm the signal. In this way, the original signal strength may get affected. 1-bit processing using Delta-Sigma modulation is a technique that removes noise by oversampling with a decrease in conversion rate. The decreased rate of conversion will sample a signal in real-time. One such architecture is proposed in this work.

2. LITERATURE SURVEY

The post recordation of the signals from medical implant device such as prosthetic neural control system are typically performed using digital control algorithm(s) which uses $\Delta\sum$ A/D conversion technique.

2.1 Problem Statement

The heart of any data converter lies in terms of its performance as speed, SNR, bandwidth, noise shaping. The analogue signal may undergo so many undesirable changes during its conversion process. In such a manner, noise reduction plays a major role to get back the processed signal in its original form.

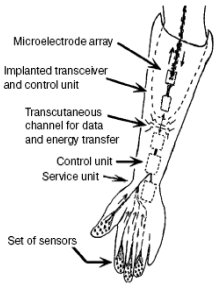

Fig 2.1 Neuroprosthesis

2.2 Proposed Method

The Delta modulation forces the quantizer successive difference between the sample values (derivative of the message signal). The feedback law will apply corrective action to the signal so that the output signal will be averaged back to the input signal level.
Thus, the output is pulse density modulated signal [1]. The strength of the signal is determined by the pulse duration of the signal. In a two-level quantizer, the output is single-bit in the form of +1 or -1.

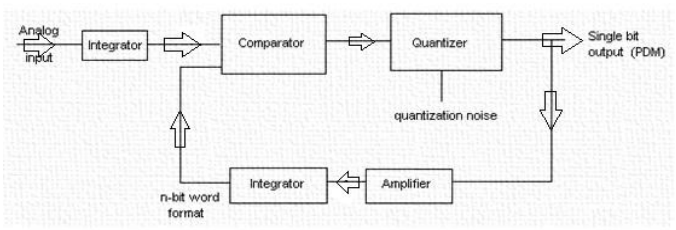

Fig. 2.2.1: Delta-Sigma Modulation [1-bit]

The demodulation process includes an integrator followed by a low-pass filter. If the integrator is simply considered as a summation process (convolution) in discrete time

form, the system is named as Delta-Sigma modulator [*Fig. 2.2.1]*.

In a precise manner, if the modulator and de-modulator section govern linear process; integrator can suitably be placed before the delta Modulator. Thus placing the integrator at the input of delta modulator gives Sigma Delta modulation [3] (Delta-Sigma modulator).

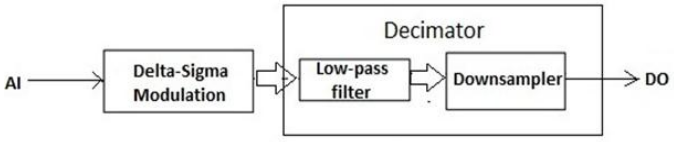

Fig. 2.2.2: Delta-Sigma Modulator

The decimation process [*Fig. 2.2.2*] is initiated by the low-pass filter (also called anti-aliasing filter) 1-bit signal (SDM output) applied to the decimator first removes the high frequency components from the base band (original message signal) that may alias into low frequency components and distort the signal. The digital low pass circuitry will be realized by a digital circuit, FIR filter or an algorithm within the signal processor.

The filtered signal which is quite above the Nyquist rate brings down by the down sampler without loss of information. Thus the Analogue input (AI) feeds the Sigma-Delta A/D modulator to get Digital Output (DO).

Conventional high-resolution converters (Nyquist) do not achieve very high speed scaled with VLSI technology. Moreover these Nyquist samplers require a complicated analogue low pass filter to limit the maximum frequency input to A/D and sample and hold circuitry.

Sigma Delta converters offer low resolution (during A/D conversion), (compromise with resolution in amplitude) noise shaping and a very high over-sampling rate. The higher resolution is achieved by the process of sample rate reduction often known as decimation. Since precise component matching is not needed for high-resolution Sigma-Delta converters, the implementation of complex monolithic systems is easier, for both analog and digital functions.

These features are not supported by conventional converter architectures, which generally require a number of high precision devices.

3. METHODOLOGY

Mathematical analysis of the Delta-Sigma structure:

The basic structure of the first order modulator is shown *Fig. 3.1*

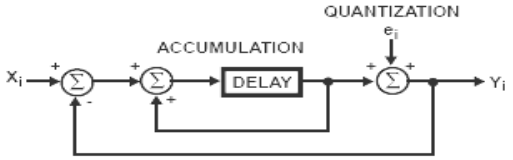

Fig. 3.1: First order modulator

The input signal x_i is compared with the predicted previous output value y_i after quantization. Any persistent difference in the signal gets accumulated in the accumulator and eventually corrects itself.

The difference equation governing fig. 5 is:

$Y_i = x_{i-1} + (e_i - e_{i-1})$ (1)

In digital domain the modulator is described as:

$Y(z) = z^{-1} X(z) + (1 - z^{-1}) E(z)$ (2)

Consider the quantization noise as uniformly distributed, uncorrelated with the input signal; the output signal [4] can be expressed as:

$$Y(z) = STF(z)\,X(z) + NTF(z)\,E(z) \quad (3)$$

where,

$$STF(z) = \frac{H(z)}{1+H(z)} = \text{constant} \quad \forall \quad z \to 1 \quad (4)$$

$$NTF(z) = \frac{1}{1+H(z)} = 0 \quad \forall \quad z \to 1 \quad (5)$$

For the first order modulator, H (z) reduces to $\frac{z-1}{1-z-1}$

Eq. (3) and (4) gives:

$$STF(z) = z^{-1} \quad (6)$$

$$NTF(z) = 1 - z^{-1} \quad (7)$$

The expression gets conformed by comparing equations (2) and (3)

The equivalent s-domain (Laplase) transfer function [2] for eq. (6) and (7) are:

$$\frac{Y(s)}{X(s)} = \frac{1}{s+1} \quad (8)$$

$$\frac{Y(s)}{E(s)} = \frac{s}{s+1} \quad (9)$$

as shown in *Fig. 3.2*

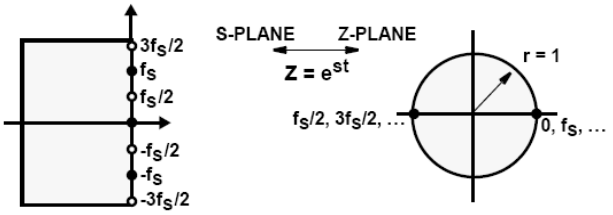

Fig.3.2 Mapping from s-z domain

Higher Order Modulators:

Extending the concept to higher order modulators

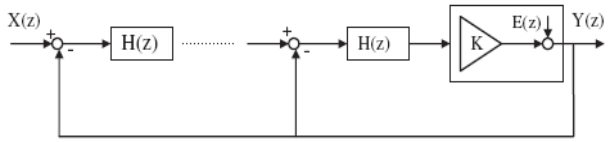

Fig: 3.3 Higher Order Modulators

At this stage, it can be stated that for a modulator of order n:

$Y(z) = z^{-n} X(z) + (1-z^{-1})^{n} E(z)$

where,

$X(z) \rightarrow$ (z-transform) x_n

$E(z) \rightarrow$ (z-transform) e_n

Equation (8) and (9) describes the behavior of Y (s) with X (s) and E(s) (Y (z), X (z) and E (z) in z domain respectively). *Fig. 3.3* highlights in general the concept of modulator of order n.

3.1 System Hardware

As the response of lower order modulators is limited in terms of noise shaping and bandwidth, the design option is to choose cascaded modulator.

The design is based on cascaded 2-1-1 (second- followed by first- follower by first order) form. For better noise shaping (set noise to higher frequencies) the filtered output from second order modulator is added with the cascade 2-1 output after digital filtering of order two. In an iterative fashion the low pass cascade 2-1 filtered signal joint with cascade 2-1-1 output followed by digital filtering of order two provides better noise shaping. The simulated output shows the behavior of the modulator. It is believed that for modulator of order greater than 4 the systems are difficult to stable.

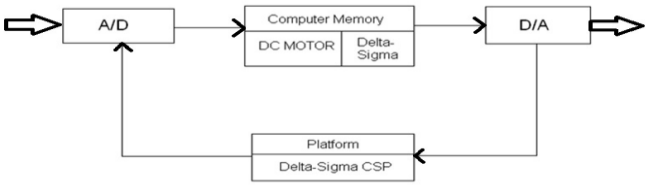

Fig:3.1.1 Delta-Sigma Control System Processor Architecture

The central idea behind designing the processor is to implement the control law and incorporate the effects of both coefficients and word length within the controller. The schematic is sketched in *Fig. 3.1.1*

All the calculations operate on 2-complement numbers, and the nature of the number is identified by the sign bit. 1 stands for negative while 0 (-1 in 1 bit structure) for positive.

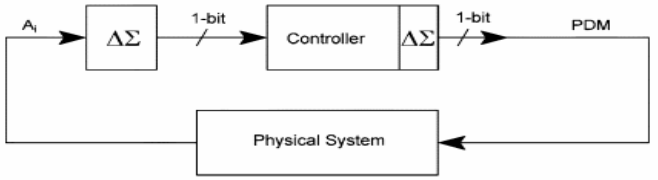

Fig.3.1.2 1-bit control scheme

The physical system to be operated upon is DC motor. The 1-bit signal in the form of PDM (pulse density modulation) or PPM (pulse proportion modulation) is sufficient to operate the DC motor.

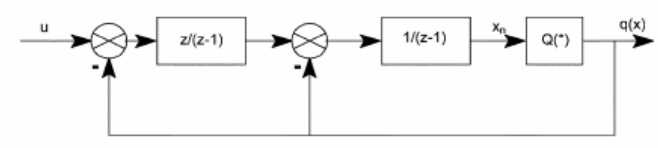

Fig. 3.1.3 Second order structure

The *Fig. 3.1.3* shows the Delta Sigma Modulation Second order structure, in which Q (x) the quantizer has, output q (x) (2-level) 1-bit PDM signal, decoded or decimated to yield Q(x) as:

$$Q(x) = \frac{1}{N} \Sigma\, q\,(x_n)_i$$

S. No.	Condition on x_n	Output q (x_n)
1	Positive or zero	+1
2	Negative	-1

TABLE-1 Quantization encoding

where, $Q(x)$ is the average value of q (x_n) over N samples. Here the case being N=1 each sample is directly related to the input x_n but with quantization noise which is q (x_n).

When OSR is much higher, $f_{s} >> f_{N,}$ q (x_n) can be ignored.
OSR = fs/f_N

1-bit processing [5] requires a very fast sampling frequency which may result in long word length for both coefficients and variables within the controller. When sampling rate becomes much higher the alternative structures as canonic δ form are used. The δ operator is defined as:

$\delta = q - 1/T$
q being the shift operator, T the sampling period.
In the limiting case (discrete structure),
$\Delta = q - 1$
And hence,
The mapping $y= \delta^{-1} x$ holds

Therefore,
y (n+1) = x (n) + y (n)
where,
controller states for the system are defined, x1 and x2.
The canonic structure is the ideal choice for the design prospects, hardware requirement, cost, spacing, memory allocation unit.
The design structure for 1-bit processing of the PDM signal [6] is:

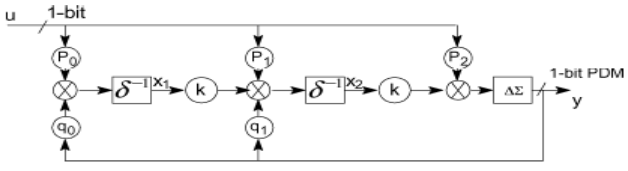

Fig.3.1.4 Canonic δ structure

3.2 System Software (Simulation)

Coefficients: Input u is a 1-bit signal from 1-bit A/D converter. Conditional negate holds as a valid technique within the controller structure.
The transfer-function of the modified δ form controller structure (4^{th} order) as:

$$\frac{Y}{U}(s) = \frac{p0k^4\delta^{-4} + p1k^3\delta^{-3} + p2k^2\delta^{-2} + pk\delta^{-1} + p4}{q0k^4\delta^{-4} + q1k^3\delta^{-3} + q2k^2\delta^{-2} + q3k\delta^{-1} + 1}$$

$$\frac{Y}{X}(s) = \frac{a1s^4 + a2s^3 + a3s^2 + a4s + a5}{s4 + b1s3 + b2s2 + b3s + b4}$$

As δ being the difference operator approximates to *sT*,
Assuming, u as an approximation of x, the coefficients within the structure of the controller are calculated as:
$p0 = a5T^4k^{-4}$
$p1 = a4T^3k^{-3}$
$p2 = a3T^2k^{-2}$
$p3 = a2Tk^{-1}$
p4=a1
$q0 = b4T^4k^{-4}$
$q1 = b3T^3k^{-3}$
$q2 = b2T^2k^{-2}$
$q3 = b1Tk^{-1}$
k = 2; as there are two levels.

The performance of 1-bit processing and ΔΣ-CSP in real time control applications is explained by the consideration of simple example of a DC motor [7].

$$H(s) = \frac{0.0001s^4 + 0.001s^3 + 0.25s^2 + 0.2501s + 0.001}{0.0001s^4 + 0.001s^3 + 0.11s^2 + s}$$

***Sampling frequency** = 1-sec (depends on SNR)*

Coefficients determination

P0 = 0.625	q0 = 0
P1 = 313.75	q1 = 125
P2 = 625	q2 = 275
P3 = 5	q3 = 5
P4 = 1	q4 = 1

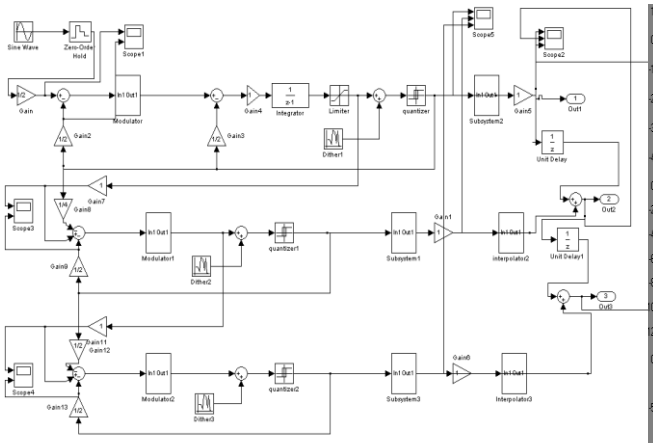

Fig. 3.2.1 Simulated Model

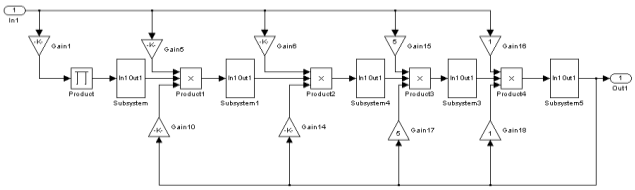

Fig.3.2.2 Controller 4th order (Both coefficients and variables)

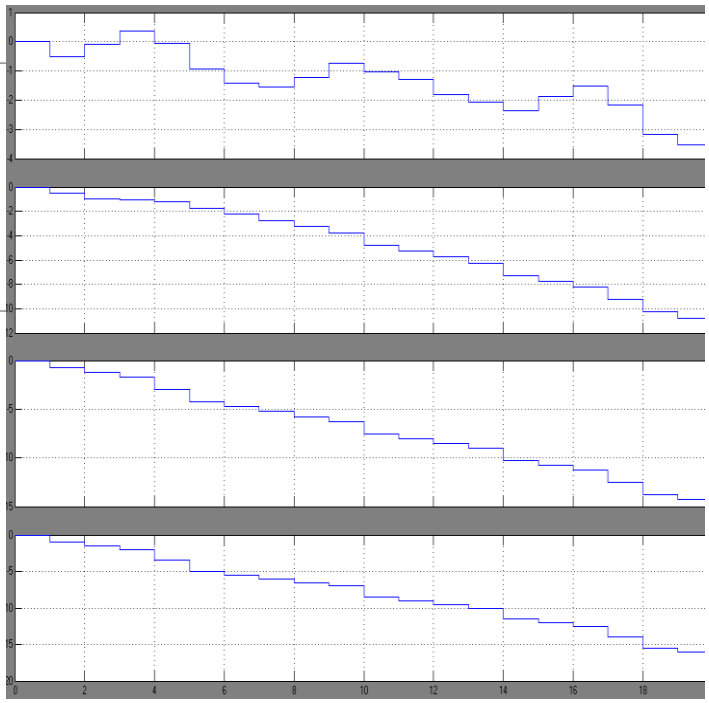

Fig 4.2: Modulator Output (first second and higher order)

4. RESULTS AND DISCUSSION

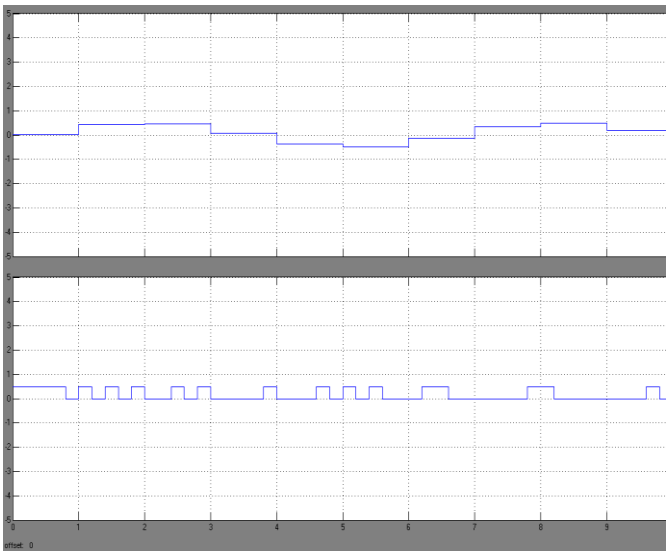

Fig 4.1: ZOH and feedback signal (1-bit format)

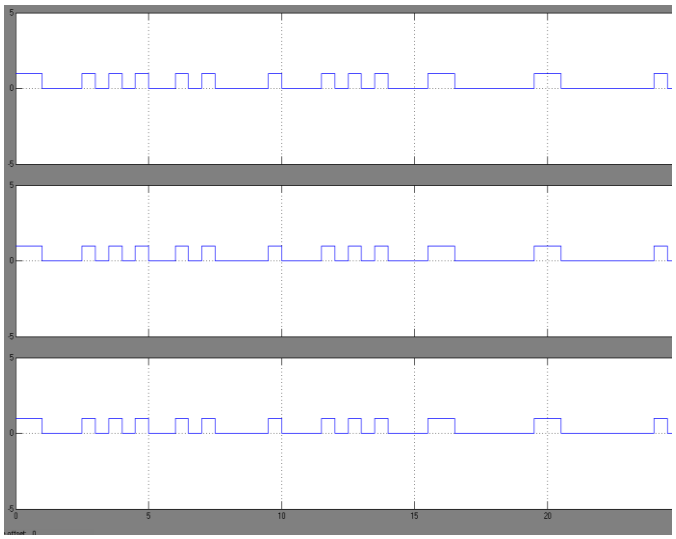

Fig 4.3 Input to the controller

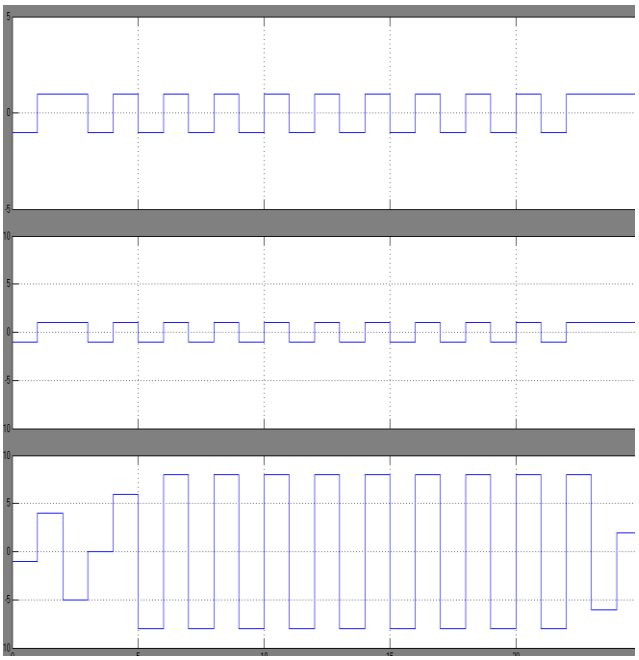

Fig 4.4 Output from controller (1-bit form)

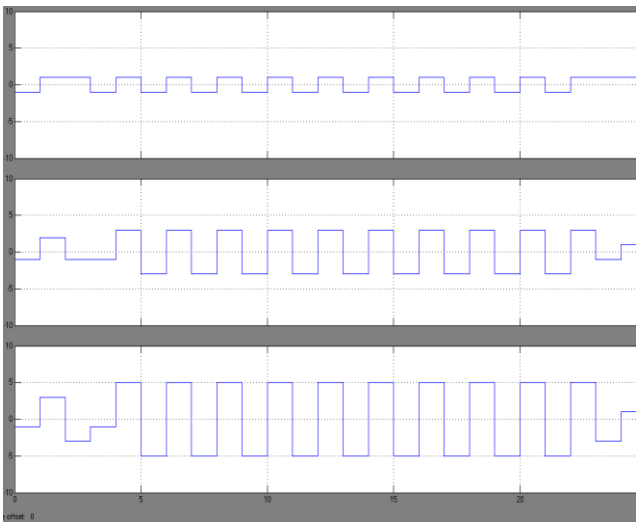

Fig 4.5 Demodulated Output.

5. CONCLUSION

The physical system is 4th order industrial DC motor. The coefficients of the controller have been determined.

The graph above shows the simulated results from ZOH, feedback signal, modulator output, controller input, controller output and demodulated output. The nature of the graph shows the behavior of the system. It can be shown that the system operates in real time upon the application of input wave.

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